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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/612,889	07/03/2003	Harish R. Devanagondi	03311.0001U3	7012

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EXAMINER	
WU, JIANYE	
ART UNIT	**PAPER NUMBER**
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/612,889	DEVANAGONDI ET AL.	
	Examiner	Art Unit	
	JIANYE WU	2616	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 February 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-6,8-18,20 and 21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6,8,10-18,20 and 21* is/are rejected.

7)☒ Claim(s) *9* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *11/25/03* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendments/Arguments

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 2/16/08 has been entered.

2. Applicant's arguments with respect to claims 1-6, 8-18, 20-21 have been considered but are moot in view of the new ground(s) of rejection due to the fact that all independent claims have been amended.

Drawings Objections

FIG 2-3, 5-7, 9A-9H, 10A-10D include informal handwritten symbols or lines that are improperly drawn. Appropriate correction is required.

Claim Objections

3. **Claim 9** is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and

> the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in Graham v. John Deere Co., 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

> 1. Determining the scope and contents of the prior art.
> 2. Ascertaining the differences between the prior art and the claims at issue.
> 3. Resolving the level of ordinary skill in the pertinent art.
> 4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

5. **Claims 1-6, 8, 10-18** and **20-21** are rejected under 35 U.S.C. 103(a) as being unpatentable over Nakayama et al. (US 6907001 B1, hereinafter **Nakayama**) in view of Rosen, IETF RFC 3031, "MPLS Architecture", January, 2001 (hereinafter **RFC3031**), further in view of Chong et al (US 20040028067 A1, hereinafter **Chong**).

For **claim 1**, Nakayama discloses in a multi-slice network processor system (FIG. 1) comprising a plurality of processing slice modules, each module processing and storing a slice of packet data, a method for processing a packet in packet slices for transfer over a network interface comprising:

assigning a packet identifier (identification filed in IP packet header, line 34 of Col. 4) to the packet;

segmenting data of the packet into cells, the data including both header and body data for the packet (lines 34-35 of Col. 4);

generating cell descriptive information (82 of FIG. 14b) for each cell, the cell descriptive information including the packet identifier, and a packet position indicator indicating an order position of data of the cell with respect to the packet (82 of FIG. 14b;

notice that fields in cell header can be used to store the cell descriptive information in any way needed); and

delivering one or more cells of the packet to one or more processing slice modules based upon load balancing criteria (QoS processor, line 56 of Col. 1);

storing one or more cells in a buffer in the packet slice (a cell must be stored in a buffer for header updating).

Nakayama **is silent on** prepending a system header to the packet, the system header providing information for use by the multi-slice system; and

generating a buffer correlation data structure correlation the buffer of the packet slice to the packet, wherein the buffer correlation data structure is a linked list of buffer identifiers

RFC3031 teaches prepending a label to each packet (lines 1-4 of Section 3.1). The information on how the local system would process the packet is provided via the label (therefore, the label is equivalent to the system header);

Chong discloses using a linked list data structure to present a packet ("link-list data structure for queuing and de-queuing packets", col. 1, line 58-59).

Using label has many advantages, including reducing the complexity (first item of Page 4 of Nakayama) of packet processing and flexibility (second item of Page 4 of Nakayama); while using a linked list to store packets us a common in the art (col. 1, line 58-59 of Chong).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time of the invention to use RFC3031 and Chong to modify Nakayama to use label

as the system header due to benefit of reducing the complexity of packet processing and performance enhancement and to using a linked list to store packets in order to quickly access to the packet data and to efficiently use memory.

As to **Claim 2**, Nakayama, RFC3031 and Chong in combination disclose the method of claim I, Nakayama further discloses wherein load balancing criteria includes that no load balancing is in effect (bypass QoS processor in line 56 of Col. 1; or configure QoS processor in a way that it does nothing to traffic).

As to **Claim 3**, Nakayama, RFC3031 and Chong in combination disclose the method of claim 1, Nakayama further discloses wherein the packet identifier is a sequence number (identification filed in IP packet header, line 34 of Col. 4) representing an order of the packet in a communications flow and further comprising assigning a communications flow indicator to the cell descriptive information of each cell of the packet.

As to **Claim 4**, Nakayama, RFC3031 and Chong in combination disclose the method of claim 1, Nakayama further discloses wherein the cell descriptive information further comprises a slice position indicator (identification filed in IP packet header, line 34 of Col. 4) indicating an order position of the data of the cell with respect to a slice of data of the packet.

As to **Claim 5**, Nakayama, RFC3031 and Chong in combination disclose the method of claim 3, Nakayama further discloses the method comprising delivering body data of the packet to one or more of the processing slices ahead of the header data of the packet (out of order is implied by lines 47-48 of Col. 8).

As to **Claim 6**, Nakayama, RFC3031 and Chong in combination disclose the method of claim 4, Nakayama further discloses the method comprising:

performing lookup functions for each slice of data (suggested by combination of 80 and 82 in FIG. 14b);

determining a size of data change in header data (suggested by combination of 80 and 82 in FIG. 14b); and

Communicating the size of data change to a queue manager via an indicator in the system header (suggested by combination of 80 and 82 in FIG. 14b).

As to **Claim 8**, Nakayama, RFC3031 and Chong in combination disclose the method of claim 1.

Nakayama does not explicitly disclose the method comprising generating a slice correlation data structure based on packet reference pointing to the buffer of the packet slice including the first cell of the packet.

Chong discloses a slice correlation data structure based on packet reference pointing to the buffer of the packet slice including the first cell of the packet ("a two-dimensional link list data structure for use in queuing and de-queuing packets", col. 3, line 17-30, or FIG. 6-14).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time of the invention to use a slice correlation data structure based on packet reference pointing to the buffer for the benefit of fast packet look-up (col. 2, line 20-22 of Chong).

As to **Claim 10**, Nakayama, RFC3031 and Chong in combination disclose the method of claim 1.

Nakayama is silent on the method further comprising: generating a slice correlation data structure for the packet including a packet reference pointing to the buffer of the packet slice including the first cell of the packet, and a respective buffer indicator for the buffer in each packet slice storing the first cell in the slice for the packet; entering the slice correlation data structure as a single queue entry into a queue.

Chong teaches generating a slice correlation data structure for the packet including a packet reference pointing to the buffer of the packet slice including the first cell of the packet, and a respective buffer indicator for the buffer in each packet slice storing the first cell in the slice for the packet ("a two-dimensional link list data structure for use in queuing and de-queuing packets", col. 3, line 17-30, or FIG. 6-14); entering the slice correlation data structure as a single queue entry into a queue (each slice is a node of the double link list).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time of the invention to use a slice correlation data structure based on packet reference pointing to the buffer for the benefit of fast packet look-up (col. 2, line 20-22 of Chong).

As to **Claim 11**, Nakayama, RFC3031 and Chong in combination disclose the method of claim 1, Nakayama further discloses wherein the network interface is a switch fabric (3 of FIG. 1) and further comprising determining a destination slice across

the switch fabric for each packet slice in accordance with load balancing criteria (QoS processor, line 56 of Col. 1).

As to **Claim 12**, Nakayama, RFC3031 and Chong in combination disclose the method of claim 11, Nakayama further discloses further comprising:

for a received packet from the switch fabric, storing each cell of each packet slice of the received packet, each cell including descriptive information, in the processing slice identified in a destination slice indicator of the descriptive information (82 of FIG. 14b).

As to **Claim 13**, Nakayama, RFC3031 and Chong in combination disclose the method of claim 12, Nakayama further discloses further comprising sending an enqueue message for each packet slice identifying a storage location of the first cell of the slice (22 of FIG. 6).

As to **Claim 14**, Nakayama, RFC3031 and Chong in combination disclose the method of claim 13 further comprising:

generating a slice correlation data structure for the packet based upon the storage location, of the first cell of each slice of the packet, and the packet identifier in each cell's descriptive information;

responsive to the size of data having been changed as indicated in the indicator in the system header, determining packet size adjustment; and

entering the slice correlation data structure as a single queue entry into a queue (22 of FIG. 6, reconstruction of a slice).

As to **Claim 15**, Nakayama, RFC3031 and Chong in combination disclose the method of claim 13, Nakayama further discloses further comprising:

upon initiation of retrieval of the packet, generating a new packet identifier for the packet;

sending a dequeue message for each slice of the packet;

correlating each cell of the packet into packet form based on cell descriptive information including the packet position indicator and the slice position indicator; and

ordering the packet for transmission to an attached network based on the new packet identifier (OUT-1, FIG. 16, reconstruction of a packet).

For **Claim 16**, it is the corresponding system claim of claim 1, therefore, is rejected for the same reason as explained in claim 1 above.

As to **Claim 17**, it is the corresponding system claim of claim 2, therefore, is rejected for the same reason as explained in claim 2 above.

As to **Claim 18**, Nakayama, RFC3031 and Chong in combination disclose the system of claim 16, Nakayama further discloses wherein the network interface is a switch fabric (3 of FIG. 1), and wherein each channel communication interface comprises a port connection with the switch fabric (LI-1 to LI-n of FIG. 1).

As to **Claim 20**, it is the corresponding system claim of claim 15, therefore, is rejected for the same reason as explained in claim 15 above.

As to **Claim 21**, Nakayama, RFC3031 and Chong in combination disclose the system of claim 16, Nakayama further discloses wherein the buffer manager comprises an ingress buffer manager (16 of FIG. 2) including an ingress buffer memory space for

each processing slice, the ingress buffer memory space for storing cells received from the respective processing slice, and an egress buffer memory space (22 of FIG. 6) for each processing slice, the egress buffer memory space for storing cells received from the switch fabric for each respective processing slice.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jianye Wu whose telephone number is (571)270-1665. The examiner can normally be reached on Monday to Thursday, 8am to 7pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Seema Rao can be reached on (571)272-3174. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Jianye Wu/

Examiner, Art Unit 2616

/Seema S. Rao/
Supervisory Patent Examiner, Art Unit 2616